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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/659,183 | 09/10/2003 | Qhalid Fareed | SETI-0006 | 7471 |
| 23550 | 7590 | 06/16/2004 | EXAMINER | |
| HOFFMAN WARNICK & D'ALESSANDRO, LLC 3 E-COMM SQUARE ALBANY, NY 12207 | | | QUINTO, KEVIN V | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2826 | |

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/659,183 | FAREED ET AL. |
| | Examiner | Art Unit |
| | Kevin Quinto | 2826 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 3 November 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 18-20 is/are allowed.
- 6) Claim(s) 1,2,5-8,14 and 15 is/are rejected.
- 7) Claim(s) 3,4,9-13,16 and 17 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/10/03 + 11/3/03
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The examiner has considered the information disclosure statements (IDS) filed on September 10, 2003 and November 3, 2003. However the examiner has found a typographical error with regard to the second reference ("Low-frequency Noise in GaN-Based Field Effect Transistors" by Levenshtein et al.) on the third sheet of the IDS filed on September 10, 2003. While the IDS shows that "pp.49-65" is cited, the actual reference indicates that *pp. 1-17 is enclosed.*

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Sheppard et al. (USPN 6,316,793 B1).

4. In reference to claim 8, Sheppard et al. (USPN 6,316,793 B1, hereinafter referred to as the "Sheppard" reference) discloses a similar device. Figure 1 of Sheppard

discloses a heterostructure field effect transistor with a buffer layer (12) on a substrate (11). There is a GaN active layer (13) on the buffer layer (12). There is a composite layer (15, 16) on the active layer (13). The composite layer (15, 16) has a strain matching layer (15) made of AlInGaN (column 4, lines 26-29). There is a barrier layer (16) on the strain matching layer (15) which is made of AlGaN or GaN (column 4, lines 18-24).

5. Claims 1, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (United States Patent Application Publication US 2002/0171405 A1).

6. In reference to claims 1 and 7, Watanabe (United States Patent Application Publication US 2002/0171405 A1) discloses a similar device. Figure 2 of Watanabe discloses a heterostructure field effect transistor with a buffer layer (2) on a substrate (1). There is an active layer (3) on the buffer layer (2). There is a composite layer (4, 5) on the active layer (3). The composite layer (4, 5) has a strain matching layer (4) made of InAlGaN (p.5, paragraph 60); thus meeting the “three group III elements and N” limitation for the strain matching layer. There is a barrier layer (5) on the strain matching layer (4) which is made of AlGaN or GaN (p.5, paragraph 60); thus meeting the “at least one group III elements and N” limitation for the barrier layer.

7. With regard to claim 6, the substrate (1) is made of sapphire (p.4, paragraph 59).

8. Claims 1, 2, 5, 6, 7, 8, 14, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Saxler et al. (United States Patent Application Publication US 2004/0061129 A1).

9. In reference to claims 1 and 7, Saxler et al. (United States Patent Application Publication US 2004/0061129 A1, hereinafter referred to as the "Saxler" reference) discloses a similar device. Figures 2 and 3 of Saxler each disclose a heterostructure field effect transistor with a buffer layer (12) on a substrate (10'). There is a GaN active layer (20') on the buffer layer (12). There is a composite layer (figure 2 – 22', 24' or figure 3 – 22'', 24'') on the active layer (20'). The composite layer (22', 24' or 22'', 24'') has a strain matching layer (22' or 22'') made of AlInGaN (claims 1, 7, 12, 47, 50, and 55). There is a barrier layer (24' or 24'') on the strain matching layer (22' or 22'') which is made of AlGaN or GaN (claims 1, 7, 12, 47, 50, and 55).

10. In reference to claim 2, figure 3 of Saxler shows that there is a gate (28'') on the barrier layer (24'').

11. With regard to claim 5, figure 2 of Saxler shows that there is dielectric layer (26') on the barrier layer (24'). A gate (28') is on the dielectric layer (26'). Saxler makes it clear that the dielectric layer (26') includes Si (p.4-5, paragraph 41).

12. In reference to claim 6, Saxler discloses that the substrate of both figures 2 and 3 can be made of sapphire, SiC, AlN, GaN, AlGaN, Si.

13. In reference to claim 8, Saxler (United States Patent Application Publication US 2004/0061129 A1, hereinafter referred to as the "Saxler" reference) discloses a similar device. Figures 2 and 3 of Saxler each disclose (p. 5, paragraphs 45 and 47) a heterostructure field effect transistor with an AlN buffer layer (12) on a substrate (10'). There is a GaN active layer (20') on the buffer layer (12). There is a composite layer (figure 2 – 22', 24' or figure 3 – 22'', 24'') on the active layer (20'). The composite layer

(22', 24' or 22'', 24'') has a strain matching layer (22' or 22'') made of AlInGaN (claims 1, 7, 12, 47, 50, and 55). There is a barrier layer (24' or 24'') on the strain matching layer (22' or 22'') which is made of AlGaN or GaN (claims 1, 7, 12, 47, 50, and 55).

14. With regard to claim 14 and 15, figure 2 of Saxler shows that there is dielectric layer (26') on the barrier layer (24'). A gate (28') is on the dielectric layer (26'). Saxler makes it clear that the dielectric layer (26') is SiN (p.4-5, paragraph 41).

Allowable Subject Matter

15. Claims 18-20 are allowed.
16. Claims 3, 4, 9, 10, 11, 12, 13, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
17. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a heterostructure semiconductor device having the applicant's specified Group III nitride materials for the active layer, strain matching layer, and barrier layer which are used in a structure that has source and drain contacts on the active layer while also on the sidewalls of the strain matching layer and the barrier layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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